Chapter 15

Projects Suggested for FPGA/ASIC Implementations

We have seen how to design VLSI systems using Verilog in the previous chapters. Complete system designs were presented for some projects, such as PCI Arbiter and Discrete Cosine Transform and Quantization Processor for Video compression applications. The design complexities were up to about 120,000 gates mapped on FPGAs. We have also implemented a couple of designs as examples, using FPGA and digital input/output boards. These are Traffic Light Controller and a Real Time Clock. All the codes developed work readily on any FPGA or as an ASIC. In this chapter, a number of applications are suggested for you to design on FPGA/ASIC.

The design methodologies and Verilog codes presented for a number of project designs in the earlier chapters may be readily applied to the new projects. Some of the codes may need modifications to suit the particular application. This design approach reduces the development cycle time considerably. If it may be suggested, it would be a good idea to put various commonly used Verilog modules such as the adders, multipliers, etc., and other modules you and other design team members may develop in a library folder for ready access by all others. However, extreme care must be taken while including comments in the codes, be it Verilog or higher level languages such as Matlab, C and, in the preparation of documents for users, without which the design will be useless. Also, do not forget to include aptly commented test benches. In this connection, mention may be made that there are few websites [102] catering to this need. You may contribute as well as download Verilog/VHDL codes for some applications along with documentation.

15.1 Projects for Implementation

We have presented a number of applications in this section and classified them into various categories. These categories, by no means exhaustive, are automotives, avionics, control system applications, medical applications, and video processing applications, to name a few. Brief descriptions are also presented for some of the applications. The reader may gather more ideas and information from websites, magazines, journals, conference papers, books, newspapers, TV shows, etc.; above all use fertile imagination before undertaking any serious design. All these systems need lots of intelligence embedded in the chips being designed. Some of the applications mentioned here are already available as embedded systems,

implemented probably with 8051 family of microcontrollers or any other processors such as 8085, 6800, 68000, Arm processors, DSP processors, etc.

15.1.1 Automotive Electronics

The first group suggested is the automotive electronics. Brief descriptions of some of the applications falling in this category are as follows: We can design intelligent controller for anti-lock braking system, also called ABS. This is already in vogue in many countries. When the road is slippery and if you jam or apply brake continuously, then your vehicle is sure to skid and go out of control. With a gentle and effective pumping action on the brake, skidding can be eliminated. But manual application on the spur of the moment will not be effective since the road conditions are not known. Even professional drivers cannot stop as quickly without ABS as an average driver can with ABS. Hence, we need a controller that will monitor the road conditions and intelligently apply the brakes intermittently at the right time.

Next, we have automatic transmission. This will dispense with the application of the gear manually. Once we start the engine and engage the gear system, normally there is no need for manual changing of gear till we reach the destination. Even high flyovers can be negotiated easily. Cruise control maintains a constant speed of the vehicle at the press of a button, thereby freeing the right foot for the brake instead of the gas pedal. These are realized by embedded systems gathering enough intelligence of the road conditions and the weather conditions. Then we have curbside check in system that issues a ticket for parking vehicles.

Older cars that came with hydraulic power steering were powered by hydraulic pumps mounted on the engine running off the engine's crankshaft. This consumes a part of the power produced by the engine. The latest development, the electronic power steering (EPS), is powered by the battery and does not draw any power from the engine. Thus, all the power produced by the engine is used to propel the car rather than run the power steering pump. Wind resistance and rolling friction stretch a car's engine and its efficiency the most and prove a drag on the car's fuel efficiency. The electronic power steering involves the use of an electric motor and related electronics for providing directional control to the car. EPS systems draw power directly from the car's battery and are not dependent on the engine for doing their job. This directly translates into an improvement in fuel efficiency.

EPS systems are more dynamic than the traditional hydraulic power steering and capable of finer inputs for varying the time and amount of power assistance being offered. This means that EPS offers higher assistance during low speed travel or during a parking situation. On the other hand, EPS decreases the level of assistance as speed builds up, a feature that gives the driver firmer control over the car at all times. This also means that the electric motor does not draw power from the battery when there is no demand for assistance, such as during straight line travel. In contrast, hydraulic systems require the fluid to be kept at a constant pressure and hence suck up power from the engine, even when the car is idling.

Apart from the electric motor, the two other components of an EPS system are the control module and the torque sensor. All these components fit together on one compact unit, installed just below the upper steering column. The electric motor set to the side of the column transfers power through a reduction and worm gear. The torque sensor detects right or left direction and the crank speed or extent of torque that the driver applies to the steering wheel and transmits the data to the control module, which in turn decides the level of aid required. It also powers the motor to turn the wheels either to the right or to the left by reversing the applied voltage to the electric power unit. EPS systems are much more efficient than hydraulic counterpart even though they draw a bit of power from the engine indirectly as the alternator has to work overtime to compensate for the battery power spent by the electric motor.

Real time monitoring system for cars and vehicles shows close-quarter dangers that a driver might miss while driving. A nice road and a big fast car/truck blend well together. However, hazardous points of driving are the packed traffic, blind spots at the immediate sides and rear of the vehicle, and painful parking maneuvers. Vehicle manufacturers are working at eliminating these dangers. These problems can be completely solved by designing a video processing system that offers an integrated display of the roof-top view of the vehicle on the dashboard, clearly showing the surroundings to decide whether overtaking another vehicle or a lane change can be safely undertaken. This system is also helpful while parking and reversing out of tight spots. This system requires front, rear, and side mounted cameras to take care of the blind spots surrounding the vehicle. The projects described earlier in this category and more projects included in the following list may be undertaken for FPGA/ASIC implementation:

- Anti-lock brakes
- Automatic transmission
- Cruise control
- Digital speed measurement of passing vehicles on roads
- Electronic power steering
- Global positioning system for automobiles
- Real time monitoring system for cars and vehicles
- Vehicle parking check in systems
- Wireless remote control for automobile AC/door/lights/alarm control

15.1.2 Avionics

The next category we will consider is the avionic systems. They are systems in aircrafts, which can measure and record digitally the parameters like latitude, longitude, altitude, inside/outside temperatures, wind speed, cabin pressure, oxygen level, identify flying objects around the flying aircraft, etc. In the airports, we see lots of baggage moving to and fro. Often, passengers have trouble in locating their baggage, especially at the destination airport. A control system which receives these baggages and routes to a particular announced baggage collection place

using a sequence of conveyor belts may be designed, saving lots of trouble for passengers. Displays at strategic points starting from the passenger arrival points must guide the passengers to the place where the passenger may collect his/her baggage without any anxiety. The list of projects for this category is as follows:

- Automated baggage clearance system in airports
- Avionic systems
  - Digital altitude meter of aircraft
  - Wind pressure display of aircraft
  - External temperature and pressure display of aircraft
- Flight simulator
- Instrument landing system (air navigation in airports – landing)
- Unmanned aircraft control

15.1.3 Cameras

In the next category, we have cameras such as auto-focus cameras, which will focus all by itself, the camcorders used as a video camera in the digital domain rather than analog domain, and the digital cameras that can record short duration compressed video sequence as per MPEG 2 or MPEG 4, Part 10 formats. These are as follows:

- Auto-focus cameras
- Digital camcorders
- Digital cameras

15.1.4 Communication Systems

Any communication system which sends data over a serial channel be it wired or wireless, is susceptible to noise and, therefore, requires error correction codes. Further, the data needs to be secure, which can be accomplished by designing encryption and decryption hardware using FPGAs or ASICs. The following list gives some of the communication systems that may be designed by the reader:

- Demodulator for satellite communication
- Encryption/decryption
- Error correction codes
- Modulator for satellite communication
- Network card
- Network switches/routers
- Quadrature amplitude modulator (QAM) and demodulator
- Radar imagery system
- Submarine detector
- Wireless LAN/WAN

15.1.5 Computers and Peripherals

Low cost computer is a low cost PC costing under $200, which is Linux-based or Windows-based. However, windows operating system based PC may cost more than the Linux-based machine, unless the windows operating system prices are slashed to compete with the Linux counterpart. In order to make this project viable, an open source for manufacturing such low cost PCs will have to be created on the net, the idea being that prices of PCs should come down benefiting people. The PC may have a one GHZ processor, 128 MB RAM, 40 GB hard disk, 15-in. color monitor, 52X optical drive, a keyboard, and a mouse. The low cost PC shall support applications such as word processing, spreadsheet, presentation, web browsing, email clients, and audio–video playback, etc.

Scan pen and PC notes taker costing under $200 captures printed text at the stroke of a pen. It is useful for researchers, journalists, doctors, lawyers, and students. It can store data up to 1000 pages of text, which can be edited and stored as separate files. It captures handwriting from any paper and enables direct downloading into MS Office. It is useful for creating and saving sketches, handwritten notes, and memos in any language without requiring much knowledge of a PC. It also can send email in our handwriting and language. The above project designs along with one more are listed in the following:

- Low cost computer
- Mobile phone personal computers
- Scan pen and PC notes taker

15.1.6 Control Systems

First one in the control system category is the alarm annunciator. As the name implies, abnormal activities in industrial plants need to be announced by monitoring various engineering parameters such as low pressure, high temperature, low fuel, etc. The industries may be a power plant, a cement plant, a sugar plant, and so on. You would have seen huge control panels (at least in the TV) in various plants such as thermal and nuclear plants, which have several flashing lamps on the top of the control panels. They are annunciators. These equipments come with various flavors of ‘sequences’, well over 50, designed by a number of manufacturers around the globe. Most of these are based on microcontrollers. Therefore, it would be a good idea to design these equipments using FPGAs/ASICs. The market for this product is huge and hence ASIC based design will be viable. In addition to the above applications, many other applications for project design are listed:

- Alarm annunciator
- Ash level controller for Electrostatic precipitator
- Automatic packaging/sealing machines
- Electrostatic precipitator communication controller
- Data acquisition system
- Electrostatic precipitator (EP) controller

- Injection molding machine control
- Lift controller
- Medicine blend control machine
- Programable logic controllers
- PIC
- Quality control system
- Rapper controller
- Remote control for air conditioners
- Robot controller
- SCADA
- Simulator for EP controller
- Temperature controllers
- Machine vision
- Smart scales
- Unmanned railway line crossing
- Vending machines

15.1.7 Image/Video Processing Systems

Many interesting project designs are available for FPGA/ASIC implementation as listed towards the end of this section. We will discuss some of these projects. Digital cinema is a new technology that is poised to create a digital revolution. It enables the projection of movies simultaneously across several theaters using satellite communication. Currently, producers are unable to release new films in many centers due to the high variable cost of film prints. This is where the digital cinema comes in handy for the producers, distributors, and exhibitors. Incidentally, this gives a new lease of life to old theaters, crying for renovation. Once the renovated theaters are equipped with adequate facilities, screening of digital cinema will become a reality. The negative may be changed to HD 5 format and encrypted and put on a centralized server. It will then be up-linked to satellite. The theater concerned will receive the signals, which in turn will go into a local server, decrypted and then on to a digital projector for screening.

A major advantage of digital cinema would be the elimination of piracy. The theaters have very little expense in terms of print cost, film transportation, or other related charges. A single film can be viewed in hundreds of theaters simultaneously. Digital cinema systems, in another embodiment, will offer theater managers the facility to choose a movie from a catalog of films and download any film from anywhere through broadband internet and satellite. It will provide for transparency as distributors can login to the internet and monitor which film of his is playing in which theater and at what time. Digital cinema also supports MPEG 2 format. MPEG 4, Part 10 format may also be included.

Detailed specification for a new digital cinema format has been released by the Digital Cinema Initiative, a forum which represents Hollywood studios: Disney, Fox, Paramount, Sony pictures entertainment (erstwhile Columbia), Universal and

Warner, which have dominated the world's English language cinema since the dawn of the movies. The full technical document can be downloaded from the website:
http://www.dcimovies.com/DCI_Digital_Cinema_System_Spec_v1.pdf.
This document is a single standard for the entire process of making and showing films digitally, namely, mastering, compression, encryption, transport, storage, playback, and projection. The picture sizes can be 2048 × 1080 pixels known as '2K' format or 4096 × 2160 pixels ('4K' format).

Mobile film making is the making of a short video backed by a brief description of a favorite icon such as an old shop house in an alley that holds many memories, a vintage car, or even a childhood experience. Image and video processing systems that may be realized as FPGA or ASIC are listed in the following:

- Conversion of black and white movies to color motion pictures
- Digital camera interface
- Digital cinema
- Digital TV and digital cable TV
- Digitizer for analog NTSC/PAL/SECAM cameras
- Display interface
- H.264 codec
- JPEG codec
- JPEG 2000 codec
- Motion JPEG 2000 codec
- MPEG 1 codec
- MPEG 2 codec
- MPEG 4 codec
- MPEG 4, Part 10 or H.264 advance video coding (AVC) codec
- Object segmentation system
- Teleconferencing systems
- TV set-top boxes
- TV tuner card
- Video conference codec
- Video grabber card
- Video karaoke
- Videophone
- Video scalar
- Video spotlighting effect and other special effects creation system
- Video watermarking

15.1.8 Measuring Instruments

High precision measuring instruments are indispensable while developing systems, be they analog or digital systems. These instruments may be used for testing a finished product or for calibration of test equipments in quality control departments.

For example, a digital high voltage tester of capacity 100 KV can be used in the quality control of a transformer cubicle used in power stations. This equipment, used by control panel manufacturers, helps in finding the breakdown voltage between copper bus bars mounted on insulators and the cubicle. Another equipment the reader can design is a 3 GHz (or more) digital frequency meter that can measure frequencies of an oscillator and thereby carry out factory setting, say for instance, setting a real time clock quickly, whose design was presented in the previous chapter of this book.

Virtual instrumentation places the personal computer at the epicenter of the task and exploits graphical programing aids such that even a novice can drag and drop ready-made instrument panels which can look like the real multimeter, spectrum analyzer, or waveform generator. The virtual creation of measuring system ranges from the simple digital voltage, current meter to the most complex multisensor data acquisition system. Other creative directions of the virtual instrumentation have taken it to the embedded systems developer and the virtual electrical engineering laboratory. Standard and classical experiments on DC machines and transformers, analog and digital circuits, etc. can be virtually performed on the PC, complete with variable running speed, operation amplifiers, gates, flip-flops, counters, stunningly realistic meters and controls. Some of the measuring instruments suggested for implementation are listed in the following:

- Digital high voltage tester
- 3 GHz Digital frequency meter
- Digital LCR meter
- Digital megohmmeter
- Six digit digital multimeter
- Digital Ph meter
- Digital oscilloscope
- Embedded systems
- Virtual instrumentation using PC

15.1.9 Medical Applications

High blood pressure increases the chance of getting heart disease and kidney disease and consequent stroke. It can also result in blindness. High pressure is especially dangerous because it often has no warning signs or symptoms. Regardless of race, age, or gender, anyone can develop high blood pressure. It is estimated that one in every four American adults has high blood pressure. More or less, the same is true around the world. Once high blood pressure develops, it usually lasts a lifetime. Blood pressure is the force of blood against the walls of arteries. The pressure rises and falls during the day. If we exercise or just walk, the pressure increases even if we are normal. However, when blood pressure stays elevated over a time, it is called high blood pressure.

The medical term for high blood pressure is hypertension. A blood pressure level of 140/90 mm Hg or higher is reckoned as high. If it is within the range of

120/80 mm Hg and 139/89 mm Hg, then it means that one is likely to develop high blood pressure. The first number is called the systolic pressure and the second number is called the diastolic pressure. The systolic pressure is the force of blood in the arteries as the heartbeats, whereas the diastolic pressure is the force of blood in the arteries as the heart relaxes in between beats. Causes of high blood pressure may be due to narrowing of the arteries, a greater than normal volume of blood, heart beating faster or more forcefully than a normal beating, etc. You can prevent and control high blood pressure. The applications that may be developed are listed below along with others in the medical applications category:

- Digital acupressure
- Digital blood glucose meter
- Digital blood pressure and heart rate monitor
- Electrocardiograph
- Life-support systems
- MRI/CT scan
    - Doppler
    - Echo
    - Mamogram
    - Ultrasound

15.1.10 Miscellaneous Applications

A number of project designs for implementation are listed in this category. Some of these projects are discussed in the following. An electronic voting machine (EVM) consists of two inter-connected units: the control unit and the ballot box. The control unit is operated by the presiding electoral officer. The names and symbols of all the candidates are displayed on the top of the ballot box. There is a push button besides each name. Each machine can accommodate up to 16 names. If there are more candidates, then another machine is linked to the first unit. When a voter enters the booth where the voting machine is kept, the presiding electoral officer presses a button marked ‘Ballot’ on his control unit. A LED marked ‘Busy’ comes on in the control unit and one marked ‘Ready’ glows on the ballot unit. ‘Ready’ LED remains on till the vote is cast. When the voter presses the push button adjoining the candidate’s name of his choice, a red LED switches on besides the candidate’s name and a loud beeping alarm sounds, indicating that the voter has cast his/her vote. Once all the votes are polled, the presiding electoral officer closes a key operated switch marked ‘Close’, after which the machine automatically stops registering any votes.

An EVM is fast, with a capacity for five votes a minute. This eliminates the cost of printing ballot papers and is tamper proof. Even an illiterate voter can use it. Counting and declaration of results are quick, which means that manpower requirement is drastically cut. A single magnesium battery in the control unit powers all the linked ballot units. The machine even prevents malpractices like vote duplication. If a voter were to press more than one button at the same time, no vote is cast. On the other hand, if buttons are pressed one after another, the EVM detects

which was pressed first and registers it as the only vote. The memory lasts five years even when the machine is switched off and not in use, and so it comes handy if a result is disputed much after the poll is over.

Futuristic capsule simulator is one of the entertainment systems, which offers the excitement of spectacular fantasy worlds in one of its kind outdoor simulator.

A pedometer is a pager like device, worn on the waist to record the number of steps a person takes in a day. It translates that into the distance covered and tells how many calories the person has burned. This is a simple tool for athletes, joggers, health buffs, and people out to lose weight. The pedometer works by sensing the up and down movements of the hip and thereby counting the steps. Before that, a user needs to record the length of steps he or she takes with a measuring tape. Once that is done, the user has to key in the person's weight, and then, the user is ready to go. This may be regarded as a motivating tool to remind us to walk more and be active and is an excellent recorder for tracking our activity level throughout the day. An average person walks about 6000 steps a day, and we need to hit 10000 if we need to loose weight. One can wear it all day, everyday and record the total number of steps one takes or just wear it whenever one takes walk or go for a workout. Using it also helps one set and reach daily targets, since one can sneak in 10 min or more of walking at every opportunity, whether it is taking the dog out for a run or just taking the stairs instead of the elevator. The pedometer may gain new lease of life marketed by government officials, fast food outlets, gyms, potato chip companies, etc.

A satellite view search service allows users to zoom in on any spot on earth for a dramatic satellite eye view in three-dimension. Drawing on a huge library resource of satellite imagery, merged with cartographic information from the ground, the application provides resolutions down to one meter or less. The application works on PCs that include a 3D graphics board with resolutions of 1024 × 768 pixels or 800 × 600 pixels. Many global locations are book marked and clicking on this spins the globe and zooms down to the desired place clearly identifying all the details. Pan and tilt controls allow one to rotate the view so that the buildings can be seen in sharp 3D. Entering the latitude and longitude of any place on earth sends the application zooming to that spot at one meter or less resolution. In such areas, the user can search for motels, gas stations, bus stations, etc. The application also provides for higher resolution of graphics and links the application to a global position system (GPS) position locater, if the user has one.

A treadmill is a type of fitness equipment used in gymnasiums. It is attached with a 3 HP motor that gives a speed between 1 to 12 miles per hour with five speed profiles and five intensity levels. To increase the intensity of training, the treadmill has an electric inclination system. The treadmill is designed with an integrated double fan, extra wide, and long shock absorbing running track with auto-safety key and hand rail bottoms for comfortable and safe training. Heart rate control, body fat control, system, telemetric pulse control, and contact pulse measurement system are a value addition to the equipment. The equipment may be designed with LCD display and the sequence of speed, inclination, and timings can be user programed. This equipment comes with six challenging programs

targeted at runners and walkers, with a provision to make more programs by the users. The list belonging to this category of applications follows:

- Automatic teller machines
- Automatic toll systems
- Digital lockers
- Digital petrol/diesel dispenser
- Dishwashers
- Dryers
- Electronic card readers
- Electronic voting machine
- Fault location in cables
- Futuristic capsule simulator
- Hearing aids
- Intelligent cane to lead the blind/deaf persons
- Leather area measurement equipment
- Non-destructive test of ceramic bricks using ultrasonic sound
- Non-destructive test of dams/buildings using ultrasonic sound
- On-board navigation
- Point-of-sale systems
- Pedometer
- Satellite view search
- Smart ovens
- Speech recognizers
- Treadmill with heart meter for gym.
- Universal PROM/PAL/FPGA programer
- Virtual reality system
- Xpendable bathy thermograph

15.1.11 Music

Separation of human voices from orchestrated music, a challenging design task, can be used to replace the original old voices by the current singer's voices while retaining the original orchestra instruments. On the other hand, the original voices can be recast in new orchestrated music. These are useful for professionals, amateur musicians, and audio karaoke. The following lists some of the musical equipments:

- Digital filter for separation of human voices from orchestrated music
- Digital voice/music recorder cum digital camera
- Special effects generators for audio:
    - Bathroom effect
    - Cave effect
    - Echo fade in/fade out effect
- Synthesizer or music keyboard

15.1.12 Office Equipments

Some of the office equipments are as follows. Digital dictaphone is a digital recorder cum player useful for secretary in an office. FAX, Scanner, Copier, and Printer can be integrated into one machine, designed as a single ASIC. Personal digital assistant is a mobile unit to store telephone/cell numbers, addresses, email addresses, and other details of persons. It can be connected to a PC using USB port for downloading or uploading the information:

- Digital dictaphone
- FAX/scanner/copier/printer four-in-one machine
- Personal digital assistant (PDA)

15.1.13 Phones

Cell phones are currently distributed on two ASICs, analog and digital. Using mixed signal HDL such as the AMS CAD of Cadence, one can design a single chip cell phone, bringing down the cost. Accordingly, the base stations can also be designed. Low resolution, low frame rate videophone/video conferencing based on H.264 can be attempted on the cell phone. A short list of the phone based equipments is as follows:

- Cell phone, single chip
- Low resolution, low frame rate videophone/video conferencing based on H.264 on the cell phone
- Multi-channel TV reception on cell phone
- FM radio on cell phone
- Cell phone base station
- Satellite phone
- Telephone exchange

15.1.14 Security Systems

Systems known as biometrics reduce an image such as a fingerprint, facial feature, or other personal characteristics to a template of minutia points or other personal characteristics. Rather than use passwords, biometric devices identify people by behavior or physical characteristics like fingerprints. Notable features of these minutia points are loop in a fingerprint or the position of an eye. These points are converted to a numeric string by an algorithm and stored as templates. These templates can be dangerous if stolen. Altering biometric images enhances security, keeping hackers at bay. Researchers may develop ways to alter images in a defined, repeatable way so that hackers who managed to crack a biometric database would be able to steal only the distortion and not the original image. This is done by distorting the image before it is scanned by a biometric reader, and the template of the distorted image is stored in a database. Thereafter, when the same person

uses the biometric reader, once again the original image is distorted and transformed, creating a match with the database. It may be noted that the original image is not stored anywhere. That means, even if hackers get the altered biometric, it would be of little use as long as organizations maintained their own formulas for transforming images before scanning.

Home security systems primarily have passive infrared motion detector, which detects infrared radiations from an intruder. It then triggers an alarm loud enough to alert the occupants of the house/office and even neighbors. The system consists of a control panel and communicatively coupled to various sensors installed in a house/office/bank and a remote control with which the system can be armed or disarmed. Apart from triggering an alarm, the system can be programed to call a pre-set telephone numbers in case of a break-in. The sensors, normally attached to the doors and windows and connected to the control panel (wired or wireless), set off an alarm immediately after they detect a movement when the intruder tries to force open the doors and windows. The client's control panel can also communicate round-the-clock with a central monitoring police station. Optionally, the system can have a closed circuit TV. Some of the security systems are as follows:

- Biometrics such as fingerprint identifiers
- Fire alarm system
- Home security systems
- Surveillance camera control system
- Theft tracking system
- Tsunami warning system

15.1.15 Toys and Games

Video games command an ever increasing huge market of over $20 billion worldwide, with a large untapped market in the east. Games such as car racing, star wars, boxing, asteroids, space traveling, etc. demand faster processors than what exists currently. ASIC based video games are better alternatives than the PC processors, especially in terms of processing speed and price. Game development is a multi-disciplinary field demanding diverse skills such as drawing, art design, painting, graphic designing, 3D graphics, story narration, screen writing, direction, etc. with a strong knowledge of digital video technology, HDL, computer programing using C++, physics, mathematics, etc. Video games require a plethora of hardware such as the sound cards, graphic cards, 3D graphic accelerators, joysticks, remote controls, CD drives, etc. These applications are listed as follows:

- Electronic toys
- Portable video games
- Toy robots
- Video game consoles

And the list goes on and on, limited only by one's imagination.

15.2 Embedded Systems Design

Computing systems have proliferated everywhere, so much so that we are conditioned to think only in terms of personal computers on our desktops, laptop computers, main frame computers, servers, etc. However, there is another class of computing or controlling system that is far more common. Yes, you guessed it right – the embedded systems/controllers. Again, when we speak of controllers, what pop up in our mind are the programable logic controllers (PLC) or the programable controllers that have invaded every conceivable industrial application. There is also a general impression among system designers that embedded systems mean only a microcontroller. Against this background, a formal definition for an embedded system is indeed hard to make.

In the recent years, there has been a spurt in embedded systems reported for wide variety of applications, which make use of microprocessors, microcontrollers, and DSPs right from 4 bits to 32 bits on one hand to FPGA/ASIC on the other. These applications include digital cameras, automobile automation, avionics, ATMs, cell phones, electronic toys/games, medical equipments, defense equipments, industrial controllers, etc. We have discussed a number of them in the previous section. If one scrutinizes these systems closely, one would infer that they have certain common features such as executing a single program repeatedly, having to meet tight constraints, i.e., they are characterized by low cost, low power, small, fast, etc., and continually reacting to changes in the system's environment and computing certain results in real time without delay. So long as these criteria are satisfied to the extent feasible, we may not have any objection to defining an embedded system as a system that is designed to perform only a dedicated application, no matter what processor is used.

An embedded system performs a dedicated function. For instance, a digital camera that can do only one function, namely, capture an image, bring about compression, store them, and upload the captured still images to a computer; nothing more, nothing less may be regarded as an embedded system. This embedded application is best realized as an ASIC since it finds a huge market. As another example, we may take the implementation of electrostatic precipitator controller used in thermal power plant for the disposal of ash. This controller is based on Intel's 8085 microprocessor by many leading vendors, rather than going for 8051 family microcontroller that came later. This may also be realized using FPGA and subsequently as an ASIC as it has good market potential and can compete with the existing versions. A detailed specification and architecture of this application for FPGA and ASIC implementation will be presented in Section 15.4. Most embedded systems need to be designed with built-in real time clock and/or watch dog timers. These designs were presented in earlier chapters.

Design metric is a measurable feature of a system's implementation. Common metrics are the functionality implemented, ease of handling the system, the processing time or throughput of the system, sale price of each system, non-recurring engineering (NRE) cost, the physical size of the system, the amount of power consumed by the system, and flexibility, i.e., the ability to change the functionality of

the system without incurring heavy NRE cost. Optimizing design metrics is a key challenge that needs to be addressed while designing an embedded system.

Microprocessors are used in a variety of applications, small to medium-sized in complexity. 8085, 8086, and 68000 processors are some of the earliest general purpose microprocessors used in embedded system applications. Likewise, digital signal processors (DSP) such as TMS320C6X (Texas), ADSP 21020 (Analog Devices), DSP32C (Lucent) are used for specialized applications involving multiply-accumulator (MAC) operations and are generally costlier than microprocessor-based products. Microcontrollers such as 8051, 89C52 (Atmel), 68HC811 (Motorola), PIC 16F84 microcontroller (Microchip Technology Inc., USA) are popular for small-end applications. For medium to high-end embedded systems design, FPGAs/ASICs are the right choice. In the near future, FPGAs may be expected to be cost effective even for small end applications and can outperform the above mentioned processors.

15.3 Issues Involved in the Design of Digital VLSI Systems

Any product is saleable only if it is cost effective and competitive. These requirements can be met if we build the system with minimum of hardware: both on-chip resources and the external hardware, and conform to optimum specification. If the system design is based on FPGA and requires a large memory in the order of 16 KB or more, the system is cost effective only if the memory is located external to the FPGA. This may mean a reduction of throughput since the external memory design is slower than the on-chip memory by about two times as was shown in the chapter on design of memories. As the technology is changing rapidly, the limit of on-chip memory of 16 KB can be jacked up if found cost effective. In ASIC implementation, it may be advantageous to integrate the memory with the ASIC and bring it out as a system-on-chip (SOC). This requires vendor library for memory while using the ASIC (front end and back end) development tools such as the Synopsys, Magma, and Cadence. Of course, we can go in for ASIC implementation only if there is a huge assured market and a promise of recurring demand. Otherwise, FPGA implementation is cost effective. Similarly, the system must have a requisite number of external hardware such as integrated circuits; passive and active components such as connectors, cables, resistors, capacitors, switches, relays; transistors, drivers, zener diodes, etc. with the right specifications, nothing more, nothing less as required by the particular application.

By minimizing the hardware, the system cost is kept low, consumes less power, development cycle as well as the production times are low, reliability high and the system is compact. User controls and displays must be simple and conveniently placed and the system must be designed with aesthetics in mind. Specification must be met completely without making any compromise. Otherwise, credibility is lost. Likewise, over indulgence of specification must be curtailed since it corrodes the profitability. Codes must be optimized in order to minimize the chip area and hence reduce the cost.

Before coding in HDL, the design concepts and algorithms developed must be tested in higher languages such as Matlab or C. Their end results can also serve as references for verifying the outputs of HDL codes. Development of HDL codes must be undertaken only if Matlab or C simulation is satisfactory. If not, one must look into the possibility of compromising on the specifications and get user concurrence before proceeding further. HDL codes, be it Verilog or VHDL, must conform to RTL coding guidelines discussed at length in Chapter 5, without which FPGA or ASIC implementation cannot work. Serious designers, be they practicing engineers or students working on their projects, need to use the right tools such as Modelsim, Synplify, and Place and Route which allow large designs without any restriction, besides being easy to learn and handle subsequently. It may be noted that free downloads may have restrictions of about 750 lines, while most VLSI system designs are above 1500 lines. The Verilog/VHDL codes developed must, in general, be technology independent, device as well as vendor independent so that we are free to use any device: FPGA or ASIC. This way, we have the flexibility of migrating from one FPGA to another FPGA or ASIC when the occasion demands without needing to recode.

Once the coding is completed, printed circuit board (PCB) which houses the target FPGA will have to be fabricated. Usually, this is time consuming and development costs incurred are high. A better alternative to the PCB development and testing of the assembled board is to buy suitable, populated, pre-tested FPGA and input/output boards. Once the system is proven, one can take up the PCB development work, if the demand is high. Similarly, one can start with the FPGA implementations for small to moderate demands and graduate to ASIC implementations later on for bulk production.

The following summarizes the strategy we have already adopted in designing VLSI systems in this book:

- An efficient application involves designing with minimum of internal and external hardware in addition to developing optimized codes.
- Complex algorithms and concepts must be verified for establishing viability using high level languages such as Matlab or C.
- HDL code must conform to RTL coding guidelines.
- Right tools must be used to minimize the development cycle time.
- System development can be dramatically expedited if based on bought out, populated electronic cards.

15.4 Detailed Specifications and Basic Architectures for a Couple of Applications Suggested for FPGA/ASIC Implementations

We will formulate detailed specifications and develop basic architectures for a couple of applications, which the reader may take up for implementation subsequently:

- Electrostatic precipitator controller
- JPEG/H.263/MPEG codec

15.4.1 Electrostatic Precipitator Controller – an Embedded System

Electrostatic precipitator controllers are used in fly ash disposal in a thermal power plant. Several tons of fly ash are generated, disposal of which is quite cumbersome. For example, a 210 MW thermal power plant generates about 4000 tonnes of ash everyday. If released in the air, the entire township will be covered by ash. Water stream cannot directly wash the ash away – passage will get clogged in a short time. The solution is to apply a high DC voltage in the order of 80 KV in the EP, a large chamber with electrodes all over, where the fly ash is blown in from a boiler. Ash gets attracted to negative electrode and hence tamed. Activating special hammers frees the ash, which is promptly washed away by a water stream at the bottom of the electrostatic precipitator and finally disposed of in huge ash ponds situated about 5 miles away from the power house. The special hammers need to be activated in a specific sequence in order to dislodge the ash from the electrode. These hammers are, however, controlled by another controller called Rapper controller. The DC high voltage is generated by firing a couple of thyristors configured as full-wave rectifiers. The firing circuits for these thyristors are based on pulse transformers housed in a control panel in which the EP controller unit is mounted. A small capacity transformer (30 VA), together with opto-isolated transistors identify the zero crossover and AC positive/negative swings in order to generate firing triggers for the thyristors at appropriate time. The transformer is also used to supply power to the EP controller unit.

Front fascia of electrostatic precipitator controller, made of membrane key pad, is shown in Figure 15.1. All the LED displays seen through front fascia are mounted on a FPGA board. LEDs N1 to N7 announce the status of the EP such as high voltage transformer high temperature, coolant top/bottom float level, EP controller unit supply under voltage, thyristors overload/high voltage transformer very high temperature, when voltage peak is reached and the mode 'REMOTE' or 'LOCAL' respectively. Based on these annunciations, the operator may take corrective actions. DS1 to DS4 are seven segment displays used to display the mode in which the EP may be configured, EP voltage, current, etc. DS1 displays the mode the EP is set. Function modes are as follows:

– Precipitator Current	E Precipitator Voltage
H Sparks Per Min.	Bl Peak & Valley Voltage
0 Im Limit	5 Uv Limit
1 Is Limit	6 Charge Ratio
2 S Control	7 Pulse Current Limit
3 T Control	8 Loop Gain
4 Slopes After Spark	9 Addresses
P Base charge Set	L Base Charging Current

'Bl' stands for blank space. When the EP controller is switched on, the display is '0% –' in DS2, N8 (LED on) and DS1 respectively. Up/Down DISPLAY SELECT keys may be used for changing the modes as listed earlier. Various settings in different modes are tabulated in Table 15.1. Mode '1' is set only after setting all other modes. For normal operation, the EP controller is set to '–'.

The DC high voltage of the precipitator may be switched on by pressing 'HT ON/OFF' switch. The LED N11 lights up and the DS4–DS2 display increases from 0 to 100 and remains at 100. The display increase may be expedited by pressing the 'T/O' key. The calibration of the system is as follows: Set the unit to Uv (meaning under voltage of power supply of the EP controller unit) limit mode (5) and adjust 'Is' potmeter on the front fascia so that the EP current is 0.75 A. Switch to the current mode '–' and adjust the potmeter P3 in I/O board to display 75 for the precipitator current of 0.75 A. Similarly, adjust potmeter P6 in I/O board to read 75 in 'E' mode for the precipitator voltage of 75 KV. P8 is adjusted till continuous counting takes place in the six digit electromagnetic counter and set it to slightly lesser value when the counting just stops. This counter advances by one every time a spark occurs in the electrostatic precipitator.

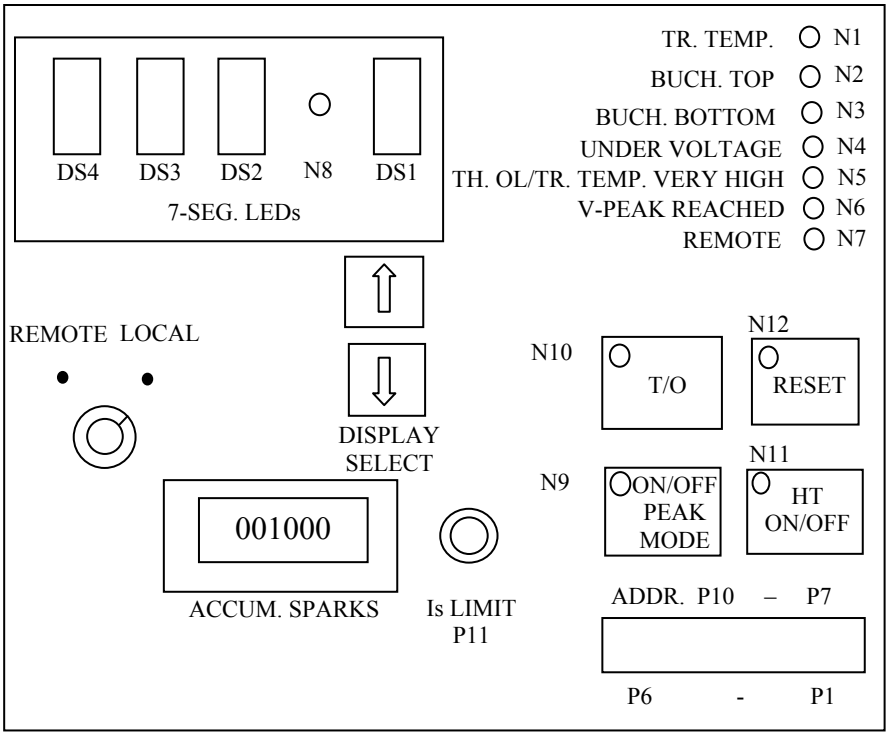


Fig. 15.1 Front panel of electrostatic precipitator controller

Table 15.1 Mode settings of the EP controller

Set mode in DS1 using Up/Down DISPLAY SELECT	Adjust potmeter (as shown in DS1) on FPGA board	Set value displayed in DS4-DS2	Check full range of potmeter setting in DS4-DS2
–	Nil	Nil	Not Applicable
E	Nil	Nil	Not Applicable
H	Nil	Nil	Not Applicable
0	0	100	0–104
2	2	5	0–25
3	3	20	0–109
4	4	30	0–99
5	5	10	0–104
6	6	1	0–31
7	7	200	0–209
8	8	20	0–99
9	9	Address in BCD switches (DS3–DS2)	
P	P	10	0–49
1	Is limit	75	0–100
L/Blank	Nil	Nil	Not applicable

Occasionally, high voltage sparks occur in the electrostatic precipitator owing to fluctuations in the flue gas flowing in the EP chamber. Peak and valley and voltage peak reached by the precipitator are required to be monitored. In the 'Peak & Valley Voltage' mode, the display DS4–DS3 shows alternately the peak and valley high voltage of the EP every 3 s. The HT voltage may be switched off by pressing 'HT ON/OFF' switch again when not required. Various potmeters and components mentioned in the foregoing description will be explained while describing the I/O and FPGA boards. Two digit BCD switches mounted on the FPGA board identify the EP controller unit. Up to 100 such controllers may be networked using serial interface circuit in the FPGA board. In the 'REMOTE' mode, only the Up/Down DISPLAY SELECT keys would be working, whereas in the 'LOCAL' mode all the keys would work.

Industrial Input/Output Board

Input/output connections and LED indicators and their partial signal conditionings are shown in Figure 15.2. Input/output board is shown in Figure 15.3. As shown in the figure, the I/O board houses signal conditioning of various analog and digital signals from the field such as sensing positive and negative AC swings, EP high voltage, EP current, sample and hold circuit to measure EP high voltage

peak, watch dog timer to restart the system automatically in the event of system getting stuck and spark sensing circuit, all of which are primarily conditioned by OP. Amps. EP high voltage is measured by sensing the current while the EP current is measured by sensing the voltage as shown in Figure 15.2. These are followed by two stage differential amplifiers with P6 and P3 potmeters for adjusting the gain of the EP high voltage and the current respectively. These analog signals are fed to a 16 channel, 8 bit ADC such as ADC0816 housed in the FPGA board. +12/–12 V supply healthiness check is also fed as one of the inputs to the ADC. All the I/Os are connected to the J3 connector.

Safety line, Contactor ON information, Buch bottom/top floats, HV transformer temperature high indication, thyristors overload or HV transformer temperature very high indication, and Alarm reset are potentially free contact inputs, signal conditioned by opto-isolators (such as CNY17-2) with 2500 V isolation. The resulting digital signals are connected to FPGA input pins. Serial input and output are connected to FPGA I/O pins via a relay and a couple of opto-isolators. HT OFF, HT ON, Warning, Tripped conditions are output using four sets of line drivers followed by one change over (1 C/O) relays. Also, a couple of SCR triggers (positive and negative) derived from FPGA are output via two numbers of 1 C/O relays.

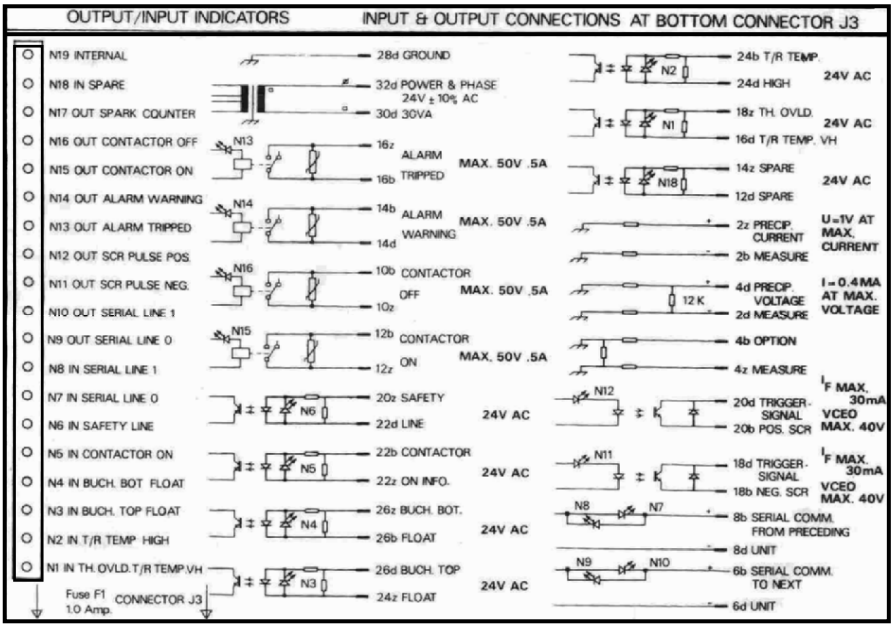


Fig. 15.2 Rear panel of electrostatic precipitator controller

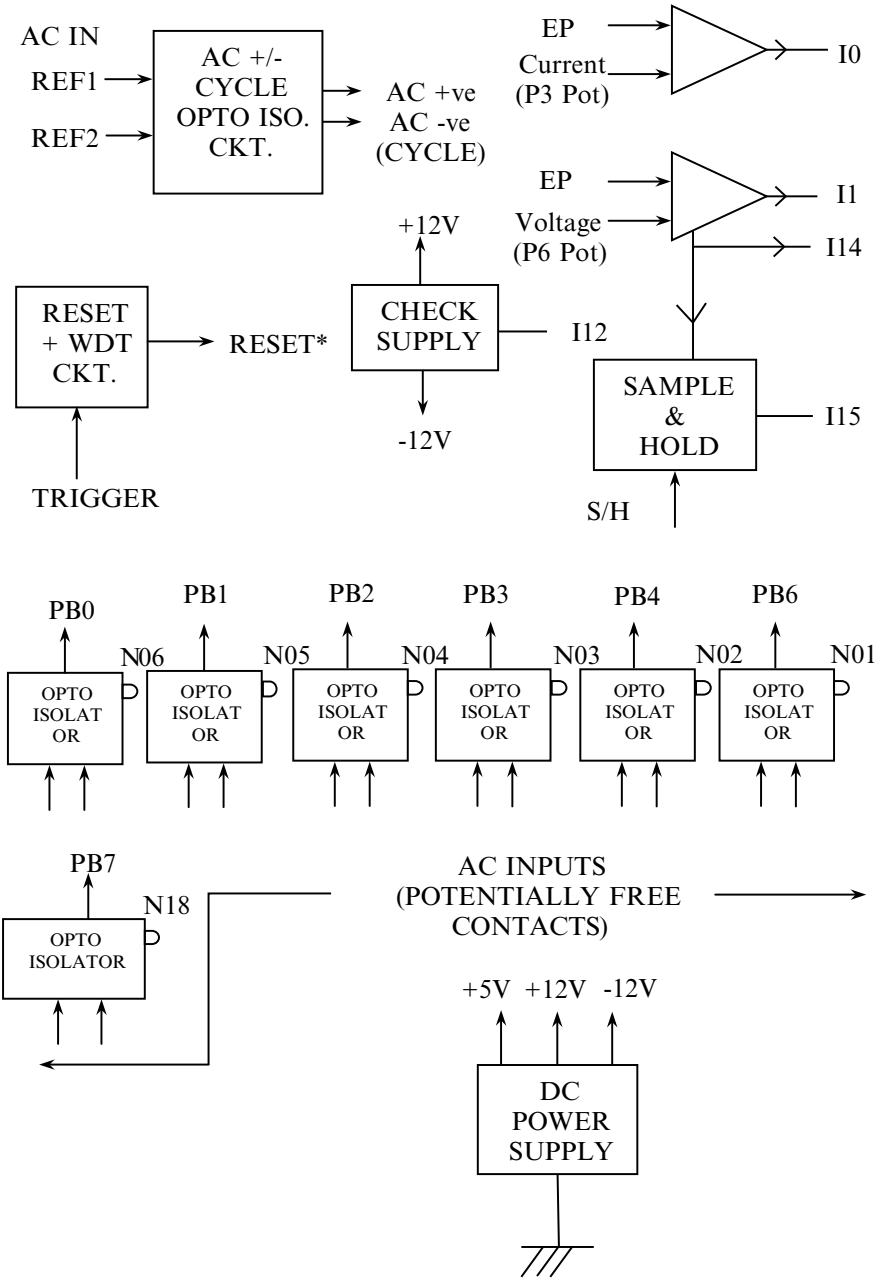


Fig. 15.3 Industrial input/output board (Continued)

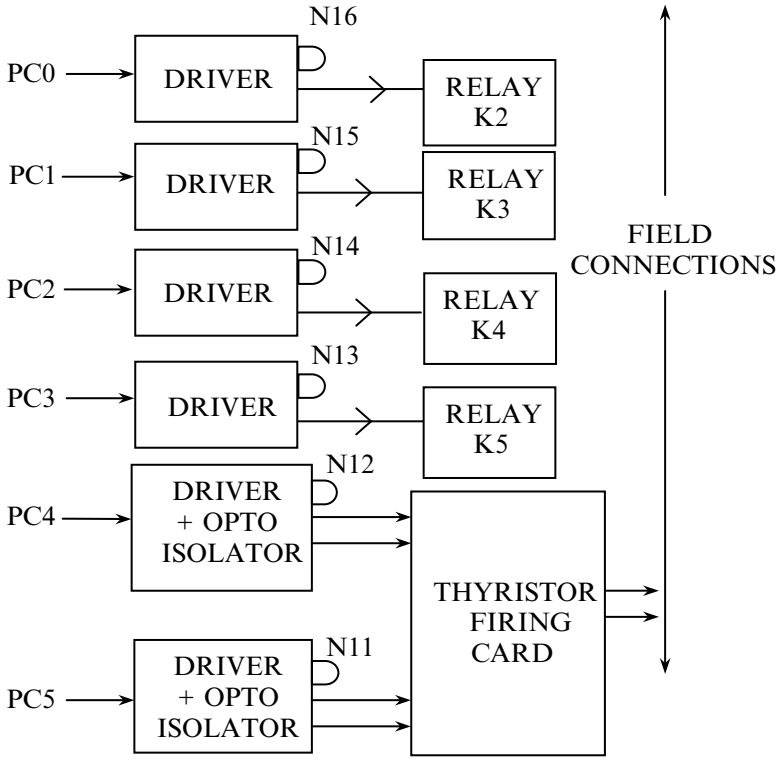


Fig. 15.3 Industrial input/output board

FPGA Board to be Designed

Electrostatic precipitator processor may be realized using a single FPGA or an ASIC as shown in Figure 15.4. Pulses AC +ve and AC –ve, signaling the positive and negative AC power swings, generated in the I/O card are fed as inputs to the device. RESET* derived from the system reset and the watch dog timer in the I/O card is connected to an input. TRIGGER is an output pulse generated by the FPGA/ASIC once every scan time of the EP controller, which triggers the watch dog timer. In the rare event of the controller loosing control owing to severe noise conditions, etc., the trigger pulse will not be generated. This in turn would reset the system and recover the normal system operation again, thus preventing system crash. Self-recovery is one of the most important characteristics in embedded systems.

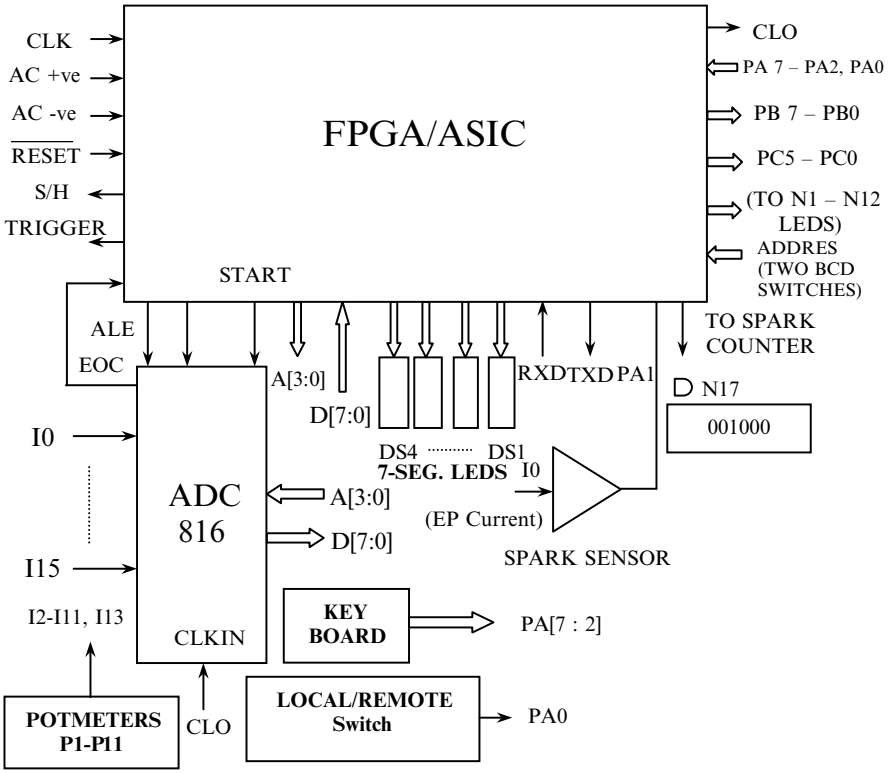


Fig. 15.4 FPGA board of the electrostatic precipitator controller

S/H output signal is asserted whenever the sample and hold is to be processed. The sampled output of I14 is fed to I15 input of an ADC 816 mounted on the FPGA/ASIC board. I1 senses the integrated EP high voltage, whereas I14 senses the dynamically changing high voltage to measure the peak or valley of the EP high voltage. I0 input of the ADC is the EP current measured by the I/O card. I2 to I11 and I13 are connected to potmeters P1 to P11 respectively shown in the front fascia. The FPGA/ASIC generates a 4-bit address, A[3:0], for the ADC to select one of the 16 analog channels I0 to I15 at a time. This address can be registered by applying 'ALE' signal. The analog to digital conversion can be initiated by asserting the 'START' signal. Once the conversion is complete, the ADC will assert 'EOC' signal. Subsequently, the FPGA/ASIC reads the converted digital channel information via D[7:0] with 'OE' asserted. The FPGA/ASIC also generates a low frequency clock, CLO, for the ADC operation.

The six key pad shown on the front fascia are connected to input ports PA[5:2] and the LOCAL/REMOTE switch to PA0. A SPARK SENSOR circuit derived from the EP current and comprising an analog comparator and a register indicates when the sparking takes place in the electrostatic precipitator through PA1 port.

DS4 to DS1 are seven segment LEDs shown in the front fascia and are connected to output ports of the FPGA/ASIC. TXD and RXD are the transmit and the receive serial data signals respectively connected to a serial network after conditioning the signals using CNY17-2 opto-isolators. PB7 to PB0 are field inputs derived from the I/O card. PC5 to PC0 are outputs from the FPGA/ASIC to drive four relays in the I/O card and the thyristors firing card. N1 to N12 are discrete LEDs shown in the front fascia driven by the output port. Another digital output advances a non-resettable six digit electromagnetic counter once every time a spark is sensed. Each EP controller unit has a unique identity by setting an 'ADDRESS' using two BCD switches. The address range is 00 to 99.

15.4.2 Architecture of JPEG/H.263/MPEG 1/MPEG 2 Codec

Video compression finds wide use in applications such as education, industries, medicine, defense, training, entertainment, sports, multimedia, desktop publishing, videophone, video conferencing, digital cameras, digital TV, digital cinema, and so on. Raw video sequences demand large storage and huge transmission channel bandwidth requirements. For example, the storage capacity required for 2 hours of raw, color motion picture of size 1024 × 768 pixels is 396 GB. Speed requirement for real time transmission of a video sequence of this size at 30 frames per second over a serial channel is 540 Mbps. Compression is, therefore, inevitable for storage and transmission of images. With a probable compression of 20 for a color motion picture in 4:2:0 format, the memory and channel speed requirements come down to manageable levels of 20 GB and 27 Mbps respectively.

High demand for these products has led to the development of various image compression techniques. Image compression methods aim at reduction in the amount of data without appreciable loss in the image quality. Design must conform to standards so that systems developed by different industries worldwide can communicate with one another. Connectivity and compatibility among different services such as videophone, video conference, MPEG 1/MPEG 2/MPEG 4 codecs are important. Standards deal with only the basic services, providing room for innovation and entrepreneurship. Several standards are available for image/video sequences:

- JPEG, JPEG 2000 for still images
- MPEG 1, MPEG 2, MPEG 4, H.264, MPEG 7 for motion pictures
- Multimedia hyper-media expert's group (MHEG)
- HDTV
- H.261/H.263 for videophone and video conferencing
  Functional modules used in standards are as follows:
    - ❖ JPEG: For still picture compression – DCT/Q/Huffman coding and their inverses
    - ❖ JPEG 2000 is also for still picture compression but uses discrete wavelet transform (DWT) – DWT, Q, bit plane coding (BPC),

binary arithmetic coding (BAC), rate control, bit stream assembly and their inverses

- H.261/H.263: For videophone/conferencing – low bit rate (p X 64 Kbps, p = 1–30)
- MPEG 1: Audio-visual codec for digital storage – transmission rate: up to 1.5 Mbps
- MPEG 2: Consumer electronics/Telecommunications/ Broadcasting – transmission rate: 2 to 100 Mbps
- MPEG 4 Part 10 also known as H.264 Advance Video Coding for mobile and broadcasting.

DCTQ/VLC and their inverses, rate control, motion estimation, and compensation are involved in H.261/H.263/MPEG 1/MPEG 2. DCTQ and IQIDCT are common to all the above standards listed except JPEG 2000 and H.264. The basic operations that bring about image compression are the DCTQ and the VLC. Still image or I frame processing employs the DCTQ and VLC, exploiting the spatial redundancy. The motion picture processing employs motion estimation and compensation in addition to DCTQ and VLC, effecting more compression owing to the exploitation of temporal redundancy.

The basic building blocks of codecs for still image compression, conforming to JPEG standards, videophone/video conference conforming to H.261/H.263 standards, and motion pictures conforming to MPEG 1/MPEG 2 standards are DCTQ/IQIDCT and variable length coder/decoder. In earlier chapters, we presented

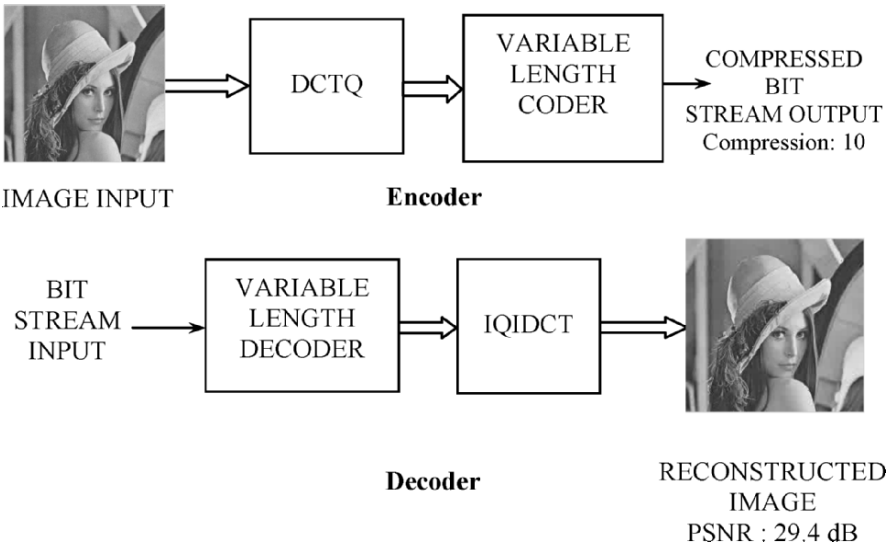


Fig. 15.5 Basic architecture of JPEG/ H.261/H.263/MPEG codec

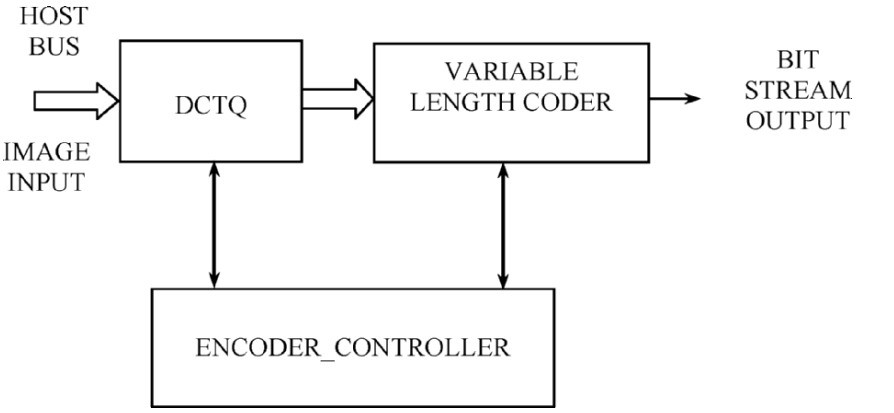


Fig. 15.6 Basic architecture of image/video encoder

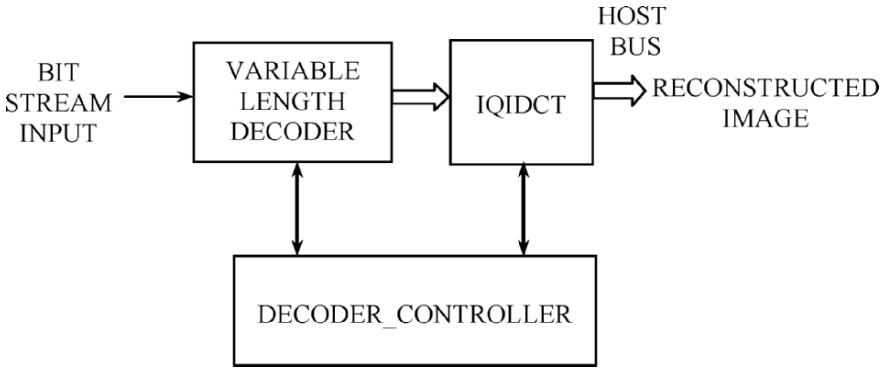


Fig. 15.7 Basic architecture of image/video decoder

the development of algorithm, architecture, and Verilog design of DCTQ. Since IQIDCT is just the inverse of DCTQ design, the design was left as an exercise for the reader. The codec for the applications mentioned earlier can be completely designed if the reader implements VLC and VLD in addition to IQIDCT modules. With these modules, the motion pictures can be processed as intra (I) frames. Those who wish to effect more compression may include the FOSS motion estimation design presented in earlier chapters or any other block matching algorithms for processing predicted (P) or bi-directionally predicted (B) frames. Detailed specification for VLC is presented in this section so that the reader may design the system without any difficulty. The reader may refer to the relevant standards [23–26] and technical papers [103, 104] before commencing the development.

The basic architecture of JPEG/H.263/MPEG codec is shown in Figure 15.5. The input image or a video sequence is applied to the DCTQ processor block-by-block resulting in quantized DCT coefficients. This is followed by the variable length coder, which assigns minimum of variable length codes, thus bringing about compression. This is at the encoder end. At the decoder end, the inverse operations take place, namely the variable length decoding, inverse quantization, and the inverse DCT. A typical compression is about 20 for a color picture in 4:2:0 format and 10 for a monochrome picture such as Lena as shown in the figure. A good quality picture can be obtained as indicated by the PSNR value of about 30 dB. The basic architectures of the video encoder and the decoder are shown in Figures 15.6 and 15.7 respectively. In addition to the modules described earlier, the encoder and the decoder modules have the encoder controller and the decoder controller respectively.

Figure 15.8 depicts the basic architecture of the implemented MPEG 2 encoder [104], capable of processing I frames. The image or the video sequence to be compressed is input block by block, by a host computer such as the Pentium, into the DCTQ processor, where the discrete cosine transform is performed followed by quantization. The input can be applied after ascertaining that READY is set. When the DCTQ processor is ready to receive the image input data, the host asserts START signal to commence the processing. The resulting quantized coefficients from DCTQ process are applied to the next stage, VLC, where they are assigned variable length codes and buffered by FIFO before they are sent out onto a serial channel as a compressed bit stream. After ensuring that VRDY is set, VSTRT may be asserted to initiate the VLC processing. EOCV indicates the completion of the process. Prior to processing the variable length codes, the header information is processed by VLC processor by writing the same into the on-chip header RAM after ensuring HRDY is set. The processing starts when the host asserts SENDH signal. The color information, Y, Cb, and Cr are input once for each macroblock.

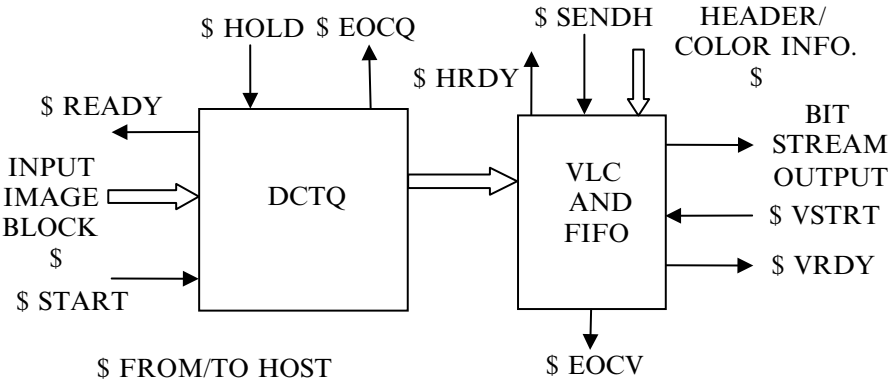


Fig. 15.8 Basic architecture of the implemented MPEG 2 encoder

On similar lines, the MPEG 2 decoder can be implemented. Details of VLC design carried out earlier are available in reference [103]. The following section describes the VLC architecture.

Variable Length Coder

A new, parallel algorithm, architecture and Verilog code for DCTQ processor were presented in Chapters 11 to 13. A video encoder that can process intra (I) frames can be developed by integrating the DCTQ processor and a variable length coder (VLC). In the following sections, architecture of a VLC featuring header information and color processing are covered.

Park and Prasanna [105] have proposed a simple and area efficient VLSI architecture for Huffman coding [106] that conforms to MPEG 1 standard. The throughput achieved with that architecture is 40 Mbps. The design implemented therein was for 8-bit symbols only, and not for a full-fledged Huffman coding whose symbol sizes can go right up to 16 bits for the DC coefficient and up to 28 bits for AC coefficients. The design is not capable of processing either the header or color information that is vital for a total working system. Being a VLSI implementation, design changes to add these features or any other modifications will be practically impossible to achieve. Naturally, this calls for a redesign.

Chang *et al*. [107] have proposed architecture for VLC encoder based on PLAs which meets the JPEG standards only. Further, the design packs the VLC code into a 24-bit constant parallel output, which eventually requires a host processor to convert the parallel information into a serial bit stream before it is sent out to the channel. As a result, the host is likely to be over burdened. Likewise, Chang and Messerschmitt [108], Lin and Messerschmitt [109], Hashermian [110], and Hsieh and Kim [111] have implemented concurrent VLC decoders. Saito [112] has implemented a real time VLC processor as a VLSI. Jeong and Jo [113] have presented an adaptive Huffman coder.

In the architecture [103] of VLC processor, the limitations cited earlier are eliminated. A cost effective, commercially available FPGA with a quick design and implementation cycle time and capable of fast design changes or modifications is made use of, unlike the implementation in Park and Prasanna [105]. The design is capable of throughputs of 50 Mbps with a 50 MHz single-phase clock and about 20:1 compression ratio on the average. The FPGA implementation meets MPEG 2 standard. The host processor is not burdened as in the case of the implementation of Chang *et al.* [107] since the implementation directly outputs the bit stream onto the channel without the need to use the host. Further, it is easy to integrate this design with the design of the DCTQ processor presented in an earlier chapter. The two processes, namely, the DCTQ and the VLC, can be pipelined.

Architecture of the VLC

DCTQ processor presented in earlier chapters prepares the ground for compression of an image or a video sequence. The next processing module is the VLC,

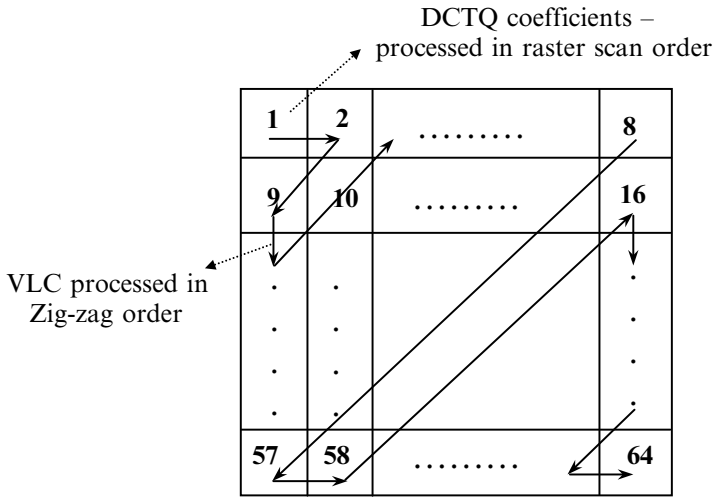


Fig. 15.9 Processing order of variable length code

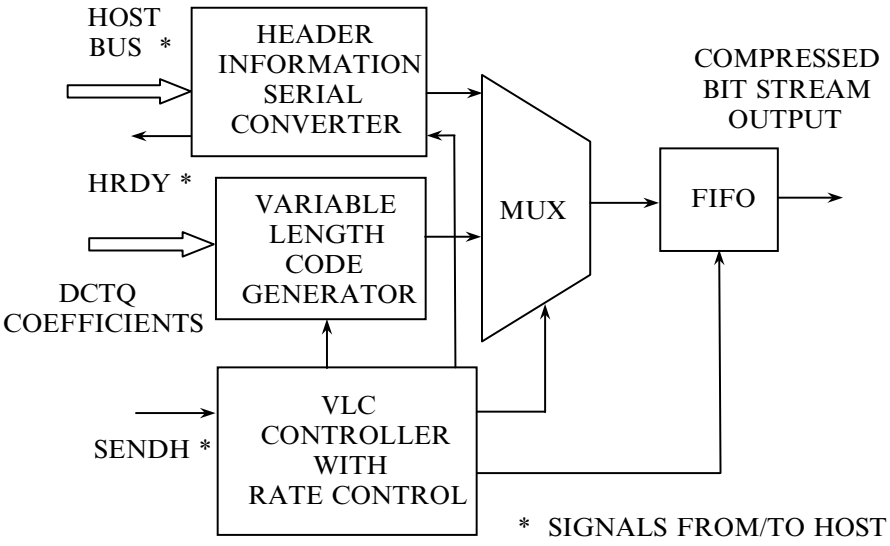


Fig. 15.10 Architecture of VLC

which assigns variable length codes to the DCTQ coefficients and transmits compressed bit stream over a serial channel. The DCTQ processor processes the DCTQ coefficients in a raster scan order, whereas the VLC processes them in a zig-zag order as shown in Figure 15.9. The basic architecture of the proposed VLC coder is shown in Figure 15.10. It essentially consists of circuitry to process header information from the host processor and to generate variable length codes from the quantized DCT coefficients, a MUX to select one of the above, a First-in–First-out (FIFO) stack to buffer the VLC output bit stream and a controller to coordinate all the sequential activities. Rate control embedded in the VLC controller maintains a constant bit rate transmission on the serial channel.

The header information containing the picture size, etc. is written by the host processor into the header RAM. A maximum of 240 bits of header information can be written into it at a time although only 129 bits per frame is required normally. The valid number of bits in the header information is also written into the header processor. The host processor can write into the header RAM only after ensuring that HRDY is set. After the host processor asserts SENDH signal, the header serial output RAM converter reads the header, byte-by-byte, using its internal counter to address the RAM. It converts the parallel information into a serial data and sends it to a MUX for onward transmission to the output FIFO.

After processing the header information, the variable length codes are generated from the quantized DCT coefficients that are input into one of the dual-redundant RAMs in the variable length code generator. RAM address is provided by the DCTQ processor. The addresses and read/write pulses required for the individual RAMs are generated or coordinated by the VLC controller. The DCTQ processor issues the end of conversion signal when it has filled all the 64 coefficients into one RAM and the same is used to start the VLC process as well. While the VLC is being processed using coefficients from one RAM bank, the DCTQ is also simultaneously processed, filling the other bank of RAM with the quantized DCT coefficients. Before commencing the VLC processing, the host processor must write into the VLC generator whether luminance (Y) or chrominance (Cb or Cr) is to be processed.

The VLC controller communicates to the VLC generator whether the DC (first RAM location) or an AC (subsequent bytes of the RAM) coefficient is being processed. The VLC generator converts each of these coefficients, read in a zig-zag sequence, into appropriate variable length codes as per JPEG/MPEG standards and sends it to the MUX as a bit stream output. After processing the DC coefficient, the same is preserved in the designated previous block registers Y, Cb, or Cr for use while processing the next block of picture. The MUX selects either the header information or the VLC bit stream using a signal issued by the VLC controller. The MUX output is fed into the next stage, the 16 Kb or higher sized FIFO, which serves as a buffer storage, before transmitting over the serial channel.

A serial output of 50 to 100 Mbps may be achieved by initiating transmission when the FIFO is about 90% full and suspending it when the content of FIFO reaches about 80% of its capacity. These limits are, however, user programable and must be experimented with actual video sequence before finalizing these set points. Rate control is incorporated in order to maintain a constant bit stream.

The VLC and the DCTQ functional modules process concurrently and have adequate interlock signals between themselves. As a result, no processing of image data will be missed. While the VLC processes image block n, the DCTQ processes (n + 1)th block. Usually, the VLC is slower than the DCTQ. Reading and writing of FIFO take place simultaneously. The VLC controller issues the end of conversion signal when the coding of the current image block is complete. If VLC is coded efficiently, it is possible to process a color motion picture of size 1024 × 768 pixels in 4:2:0 format at 30 frames per second using FPGA. A higher picture size, possibly, 1600 × 1200 pixels can be processed in ASIC implementation.

Header Serial Output Converter

This unit consists of a left shift register to convert parallel header information in RAM to a serial output and a controller to regulate various events as depicted in Figure 15.11. After making sure that HRDY is set, the SENDH signal can be asserted by the host to start the conversion. The controller addresses the header RAM using HRA[4:0] and loads the byte data into the shift register at the rising edge of CLK using the data bus, HRD[7:0] and by asserting the LD signal. An internal 4-bit counter in the controller keeps track of the number of bits to be shifted while signal LD is disabled. HRA[4:0] is incremented and the process is repeated till the entire header information in the RAM is converted into serial bits and sent out of the shift register. The total number of bits of the header information to be processed is supplied by the host. Usually, about 130 bits of header

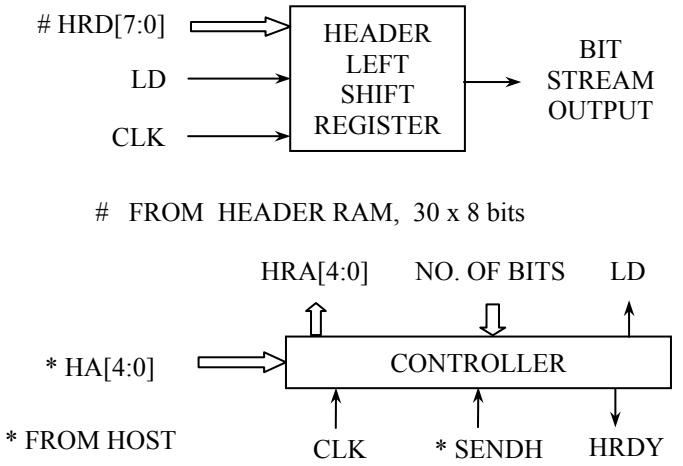


Fig. 15.11 Header serial output converter

information is transmitted per picture frame. HA[4:0] address is used by the host while writing into the header RAM and is disabled during the serial bit conversion.

VLC Generator

A simplified diagram of VLC generator is shown in Figure 15.12. It consists of a 2-bit register, C[1:0], containing the luminance or chrominance information written by the host, three 9-bit registers to store Y, Cb, and Cr DC coefficients of the previous block using the data bus, Q[8:0], a 9-bit sign-magnitude subtract circuit to get the differential DC coefficient between that of the current and the previous blocks, DC and AC VLC coders which output the variable length codes serially, a MUX to select either the DC or the AC codes, and a controller to regulate the control sequence. Which of the components: Y, Cb, or Cr is to be processed is loaded by the host before processing every macroblock.

A zig-zag counter built into the controller addresses the RAM to read the DC/AC coefficients. After processing the current DC coefficient, it is stored in one of the three previous block registers using the write signal, WR. Bit output

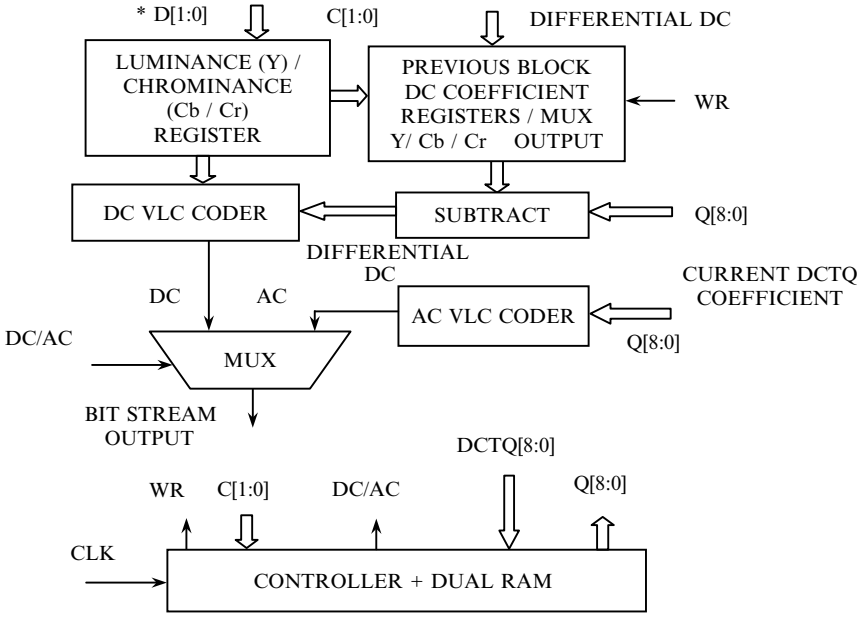


Fig. 15.12 VLC generator

from the MUX is issued once every clock cycle. The controller generates appropriate write signals, not shown in the figure, for registering the pipeline registers inside the DC and AC VLC coders.

The DCTQ or VLC, whichever process is slow, determines the overall processing time of the system since they are pipelined. It is possible to process monochrome images of size 1600 × 1200 pixels at the rate of 30 frames per second depending upon the device selected. For color images in 4:2:0 format, 50% more execution time is required than that for the monochrome picture. As a result, the maximum size of color image that can be processed will only be 67% of the size of the monochrome picture. Header processing, whose execution time is about 3000 ns is a parallel process to DCTQ and is negligible when compared to the VLC processing time of 33 ms per frame.

Oral and written presentations are very important for researchers, students, and practicing engineers. Guidelines for these presentations and a sample presentation are included in the CD. In addition, the reader is urged to develop skills in writing technical papers by studying the existing papers in the literature. A number of them can be found in the references listed in the book and in numerous websites.

Summary

Numerous project designs were suggested for implementation on FPGA or ASIC. These applications were arranged into various categories for the convenience of designers. Brief descriptions were presented for some of these projects. An introduction to embedded systems design was presented. Various issues involved in the design of Digital VLSI Systems were discussed. These were followed by the presentation of detailed specifications and architectures for a couple of projects so that the reader may straightaway start working on these projects to gain hands on experience in designing projects.

Assignments

15.1 A number of projects were suggested for FPGA/ASIC implementation in the text. Suggest some more projects for implementation for each of the following areas of applications:
Automotive electronics
Avionics
Communication
Computer products
Control engineering
Video processing

Medical applications
Miscellaneous applications
Music
Office equipments
Phones
Security systems

15.2 For each of the categories of applications you have suggested for the assignment 15.1, write a brief description.

15.3 A driver less shuttle, a light rail car, which plies between two airports at a distance of 2 miles, is to be controlled automatically. When it is waiting for the passengers at one of the stations, the two entrance/exit doors of the car must remain open. So also the corresponding doors at the station. After the car comes to a halt at a station, the car doors as well as the station doors open. In each of the stations, a push button is installed for use by the passenger(s) to request service of the car which is waiting for passengers at the other station, and has radio linked switches to detect the requests. The car leaves a station after 10 min of arrival, provided there is at least one passenger in the car at the time of departure. At the appointed time of departure, if there is no passenger in the car and, if a service request from the other station is pending, all the doors of the car and the station close, and the car departs to the other station without passengers. However, if there is no request pending, the car waits for the passengers with doors shut. When a passenger arrives, the passenger is allowed to get in and the car departs. At the time of closing, if any passenger arrives, the doors open for 5 s and close again, provided the car is not full. The entry to the car or exit from the car can be made through any of the two doors. Each of the two doors allows only one person at a time. The car can carry a maximum of 25 passengers. Draw a detailed specification of the controller and design the architecture so that the design may be coded in Verilog/VHDL RTL. State your assumptions clearly.

15.4 An alarm annunciator is a watch dog for keeping the process variables in a plant under unceasing surveillance. Usually the annunciators are mounted on the top of control panels. They keep the control engineer posted with abnormal variations in process parameters by providing visual and audible alarms, so that timely corrective action can be taken. The inputs to the alarm annunciator are potentially free, normally open (NO), or normally closed (NC) contacts. These contacts are required to be debounced. A wide variety of sequences are available depending upon the types of applications. A choice of automatic reset, manual reset, ring back, etc. are available. Three such sequences are shown in Figure A15.1. Special sequences can also be tailor-made. The visual indications are provided (to enhance the reliability) by dual-redundant, 24V, 60 mA lamps mounted on windows covered by translucent acrylic sheets. Legends are engraved on them to announce the alarm conditions prevalent at any time. Typical legends are boiler pressure high, main transformer temperature high, oil tank level low, turbine generator vibration high, excitation circuit failure, nuclear activity

high, etc., depending upon the needs of industry/plant. Typical number of windows are (expandable) 4, 8, 16, 32, etc., each servicing one control contact to monitor one plant variable. Push buttons are provided in the equipment so that the alarm may be acknowledged, reset, or tested. The visual alarms are also accompanied by audio alarms, which may be an electronic horn, whose timings of operations are shown in the figure.

Auto-alarm sequences

Sequence	Normal	Abnormal	ACK	Reset	Window	Audio 1
AA1					Off	Off
					Flashing	On
					On	Off
					Flashing	On
					On	Off
					Off	Off
					Flashing	On
AA2					Off	Off
					Flashing	On
					On	Off
					Off	Off
					On	Off
					Off	Off
					On	Off

Ring back sequence

State	Window	Audio alarm	
		Audio 1	Audio 2
Normal	Off	Off	Off
Abnormal	Fast flashing (2 Hz)	On	On
Acknowledge	Steady On	Off	Off
Normal again	Slow flashing (1/2 Hz)	Off	On
Reset	Off	Off	Off
Normal before Ack.	Fast flashing (2 Hz)	On	Off
Acknowledge	Slow flashing (1/2 Hz)	Off	On
Reset	Off	Off	Off

Fig. A15.1 Alarm annunciator (Continued)

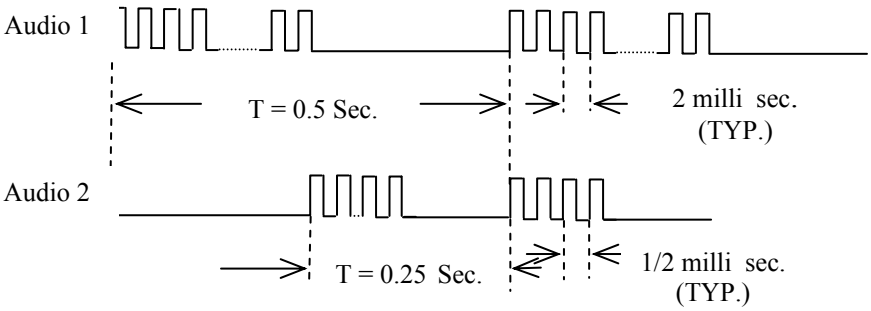
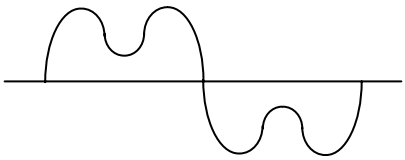


Fig. A15.1 Alarm annunciator

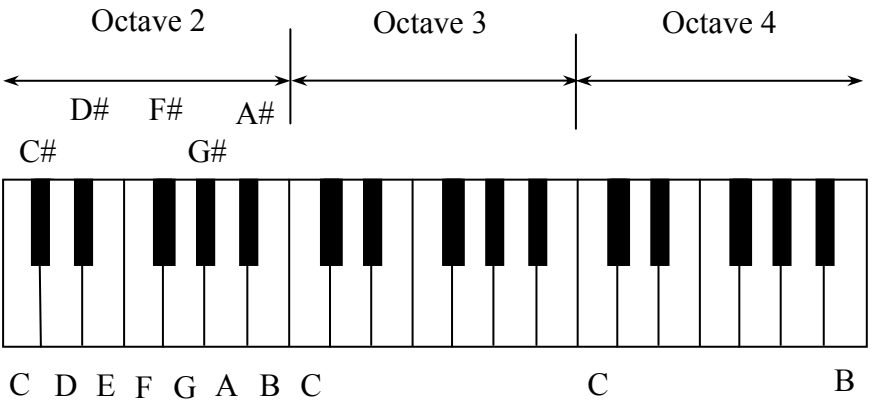
Debounce time of the contacts must be capable of being programed from 2 ms to 10 ms. Provide only one debounce time program control for all the points. Develop a detailed architecture for the annunciator such that RTL Verilog code may be implemented for 16 points or windows.

15.5 A music synthesizer is required to be designed. The output of the synthesizer is one of the musical instrument voices, whose waveform for one complete cycle is given in Figure A15.2a as an example. The waveform of an instrument voice can be manually digitized or captured using a real synthesizer for a finite time and stored in a ROM. The number of samples assumed or arrived at after experimentation must be adequate for getting good quality music. The output of the ROM must be in twos complement in order to accommodate both positive as well as the negative swings of the voice. This output is fed to a digital to analog converter such as DAC1000 of National Semiconductors in bipolar mode, which accepts offset binary (MSB of twos complement inverted) input, followed by a power amplifier and a speaker system (PA) to produce the music. PA may be assumed to be available. The key board of the synthesizer is shown in Figure A15.2b. So long as a key is pressed, the ROM must output complete cycles of the digital voice at a frequency which is marked in the keyboard diagram and the table in Figure A15.2c. If more than one key is pressed, then the highest frequency of the keys pressed is to be recognized. Develop a detailed RTL compliant architecture for the music synthesizer. Explain how you can reconfigure the entire keyboard one octave higher or lower at the flick of two push button switches. No Verilog code need be written.



a Note C at 523 Hz

Fig. A15.2 Music Synthesizer (Continued)



b Synthesizer Keyboard

Note	Frequency (Hz)	Note	Frequency (Hz)	Note	Frequency (Hz)
C	523	D#	660	F#	831
C#	554	E	698	G	880
D	587	F	740	G#	933
A	622	A#	784	B	988

The ratios of frequencies of same notes in Octave 2, Octave 3 and Octave 4 are 1:2:4.

c Frequencies of musical notes

Fig. A15.2 Music Synthesizer